Features

- Operating Range from 5V to 18V
- Baud Rate from 2.6 Kbaud up to 20 Kbaud
- Improved Slew Rate Control According to LIN Specification 2.0
- Fully Compatible with 3.3V and 5V Devices
- Dominant Time-out Function at Transmit Data (TXD)
- Normal and Sleep Mode
- Wake-up Capability via LIN Bus (90 µs Dominant)
- External Wake-up via WAKE Pin (130 µs Low Level)
- Control of External Voltage Regulator via INH Pin
- Very Low Standby Current During Sleep Mode (10 µA)
- 60V Load Dump Protection at LIN Pin (42-V Power Net)
- Wake-up Source Recognition
- Bus Pin Short-circuit Protected versus GND and Battery
- LIN Input Current < 3 µA if V_{BAT} Is Disconnected
- Overtemperature Protection
- High EMC Level
- Interference and Damage Protection According to ISO/CD 7637
- ESD HBM 6 kV at LIN Bus Pin and Supply VS Pin

LIN Transceiver

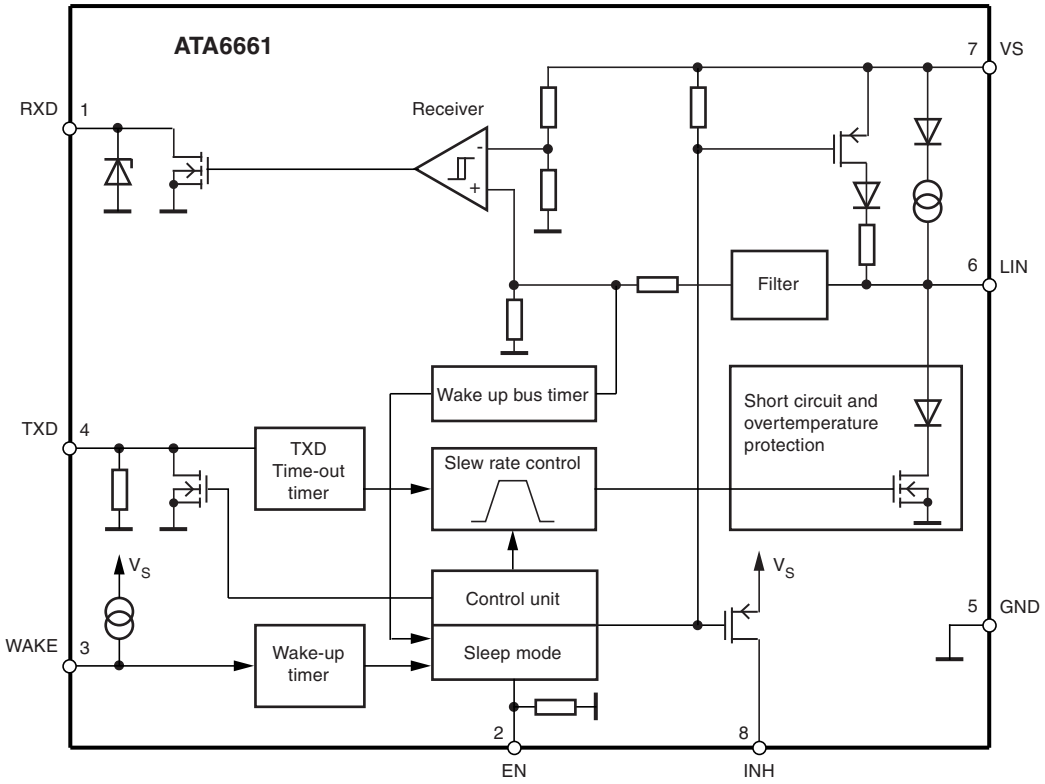
ATA6661

1. Description

The ATA6661 is a fully integrated LIN transceiver according to the LIN specification 2.0. It interfaces the LIN protocol handler and the physical layer. The device is designed to handle the low-speed data communication in vehicles, e.g., in convenience electronics. Improved slope control at the LIN bus ensures secure data communication up to 20 kBaud with an RC-oscillator for protocol handling. In order to comply with the 42-V power net requirements, the bus output is capable of withstanding high voltages. Sleep mode guarantees minimal current consumption.

4729M–AUTO–02/09

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SO8

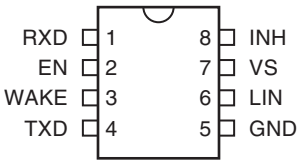


Figure 2-2. Pin Description

Pin	Symbol	Function
1	RXD	Receive data output (open drain)
2	EN	Enables normal mode, when the input is open or low, the device is in sleep mode
3	WAKE	High voltage input for local wake-up request
4	TXD	Transmit data input; active low output (strong pull-down) after a local wake-up request
5	GND	Ground
6	LIN	LIN bus line input/output
7	VS	Battery supply
8	INH	Battery related inhibit output for controlling an external voltage regulator; active high after a wake-up request

3. Functional Description

3.1 Supply Pin (V_S)

Undervoltage detection is implemented to disable transmission if V_S is falling to a value below 5V to avoid false bus messages. After switching on V_S the IC switches to pre-normal mode and INHIBIT is switched on. The supply current in sleep mode is typically 10 µA.

3.2 Ground Pin (GND)

The ATA6661 is neutral on the LIN pin in case of a GND disconnection. It is able to handle a ground shift up to 3V for V_S > 9V.

3.3 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown as well as an internal pull-up resistor according to LIN specification 2.0 are implemented. The voltage range is from –27V to +60V. This pin exhibits no reverse current from the LIN bus to V_S, even in case of a GND shift or V_{Batt} disconnection. The LIN receiver thresholds are compatible to the LIN protocol specification.The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope controlled. The output has a short circuit limitation. This is a self adapting current limitation; i.e., during current limitation as the chip temperature increases so the current reduces.

3.4 Input Pin (TXD)

This pin is the microcontroller interface to control the state of the LIN output. TXD is low to bring LIN low. If TXD is high, the LIN output transistor is turned off. In this case, the bus is in recessive mode via the internal pull-up resistor. The TXD pin is compatible to a 3.3V and 5V supply.

3.5 TXD Dominant Time-out Function

The TXD input has an internal pull-down resistor. An internal timer prevents the bus line from being driven permanently in dominant state. If TXD is forced low longer than t_{dom} > 6 ms, the pin LIN will be switched off to recessive mode. To reset this mode switch TXD to high (>10 µs) before switching LIN to dominant again.

3.6 Output Pin (RXD)

This pin reports to the microcontroller the state of the LIN bus. LIN high (recessive) is reported by a high level at RXD, LIN low (dominant) is reported by a low voltage at RXD. The output is an open drain, therefore, it is compatible to a 3.3V or 5V power supply. The AC characteristics are defined with a pull-up resistor of 5 kΩto 5V and a load capacitor of 20 pF. The output is short-current protected. In unpowered mode (V_S = 0V), RXD is switched off. For ESD protection a Zener diode is implemented with V_Z = 6.1V.

3.7 Enable Input Pin (EN)

This pin controls the operation mode of the interface. If EN = 1, the interface is in normal mode, with the transmission path from TXD to LIN and from LIN to Rx both active. If EN = 0, the device is switched to sleep mode and no transmission is possible. In sleep mode, the LIN bus pin is connected to V_S with a weak pull-up current source. The device can transmit only after being woken up (see next section “Inhibit Output Pin (INH)”).

During sleep mode the device is still supplied from the battery voltage. The supply current is typically 10 µA. The pin EN provides a pull-down resistor in order to force the transceiver into sleep mode in case the pin is disconnected.

3.8 Inhibit Output Pin (INH)

This pin is used to control an external switchable voltage regulator having a wake-up input. The inhibit pin provides an internal switch towards pin V_S. If the device is in normal mode, the inhibit high-side switch is turned on and the external voltage regulator is activated. When the device is in sleep mode, the inhibit switch is turned off and disables the voltage regulator.

A wake-up event on the LIN bus or at pin WAKE will switch the INH pin to the V_S level. After a system power-up (V_S rises from zero), the pin INH switches automatically to the V_S level. The R_{DSon} of the high-side output is < 1 kΩ

3.9 Wake-up Input Pin (WAKE)

This pin is a high-voltage input used to wake-up the device from sleep mode. It is usually connected to an external switch in the application to generate a local wake-up. If you do not need a local wake-up in your application, connect pin WAKE directly to pin VS. A pull-up current source with typically –10 µA is implemented. The voltage threshold for a wake-up signal is 3V below the VS voltage with an output current of typical –3 µA.

Wake-up events from sleep mode:

- LIN bus
- EN pin
- WAKE pin

Figure 3-1 on page 6, Figure 3-2 and Figure 3-3 on page 7 show details of wake-up operations.

3.10 Mode of Operation

1. Normal mode
   This is the normal transmitting and receiving mode. All features are available.
2. Sleep mode
   In this mode the transmission path is disabled and the device is in low power mode. Supply current from V_{Batt} is typically 10 µA. A wake-up signal from the LIN bus or via pin WAKE will be detected and switches the device to pre-normal mode. If EN, then switches to high, normal mode is activated. Input debounce timers at pin WAKE (t_{WAKE}), LIN (t_{BUS}) and EN (t_{sleep},t_{nom}) prevent unwanted wake-up events due to automotive transients or EMI. In sleep mode the INH pin is floating. The internal termination between pin LIN and pin V_S is disabled to minimize the power dissipation in case pin LIN is short-circuited to GND. Only a weak pull-up current (typical 10 µA) between pin LIN and pin V_S is present.
3. Pre-normal mode
   At system power-up, the device automatically switches to pre-normal mode. It switches the INH pin to a high state, to the V_S level. The microcontroller of the application will then confirm the normal mode by setting the EN pin to high.
4. Unpowered mode
   In this mode the LIN transceiver is disabled. Data communication is switched off. If V_S is higher than V_{Sth} undervoltage threshold, the IC mode change from Unpowered to Pre-normal mode.

3.11 Remote Wake-up via Dominant Bus State

A falling edge at pin LIN, followed by a dominant bus level maintained for a certain time period (t_{BUS}), results in a remote wake-up request. The device switches to pre-normal mode. Pin INH is activated (switches to V_S) and the internal termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller (see Figure 3-2 on page 7). The voltage threshold for a wake-up signal is 3V below the VS voltage with an output current of typical –3 µA.

3.12 Local Wake-up via Pin WAKE

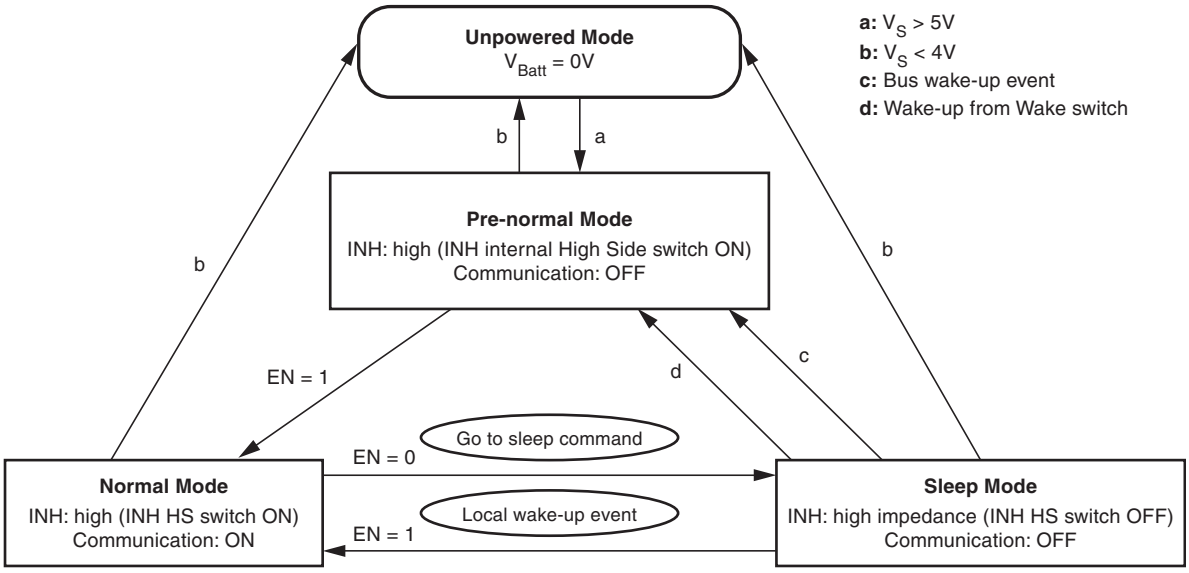
A falling edge at pin WAKE, followed by a low level maintained for a certain time period (t_{WAKE}), results in a local wake-up request. The extra long wake-up time (t_{WAKE}) ensures that no transient, according to ISO7637, creates a wake-up. The device switches to pre-normal mode. Pin INH is activated (switches to V_S) and the internal termination resistor is switched on. The local wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller and a strong pull-down at pin TXD (see Figure 3-3 on page 7).

3.13 Wake-up Source Recognition

The device can distinguish between a local wake-up request (pin WAKE) and a remote wake-up request (dominant LIN bus). The wake-up source can be read on pin TXD in pre-normal mode. If an external pull-up resistor (typically 5 kΩ) on pin TXD to the power supply of the microcontroller has been added, a high level indicates a remote wake-up request (weak pull-down at pin TXD) and a low level indicates a local wake-up request (strong pull-down at pin TXD).

The wake-up request flag (signalled on pin RXD) as well as the wake-up source flag (signalled on pin TXD) are reset immediately, if the microcontroller sets pin EN to high (see Figure 3-2 on page 7 and Figure 3-3).

Figure 3-1. Mode of Operation



3.14 Fail-safe Features

- There are now reverse currents < 3 µA at pin LIN during loss of V_{BAT} or GND. Optimal behavior for bus systems where some slave nodes supplied from battery or ignition.
- Pin EN provides pull-down resistor to force the transceiver into sleep mode if EN is disconnected.
- Pin RXD is set floating if V_{BAT} is disconnected.
- Pin TXD provides a pull-down resistor to provide a static low if TXD is disconnected.
- The LIN output driver has a current limitation and if the junction temperature T_j exceeds the thermal shut-down temperature T_{off} the output driver switches off.
- The implemented hysteresis T_{hys} enables the LIN output again after the temperature has been decreased.

3.15 Physical Layer Compatibility

Since the LIN physical layer is independent from higher LIN layers (e.g. LIN protocol layer), all nodes with a LIN physical layer according to this revision can be mixed with LIN physical layer nodes, which are according to older versions (i.e. LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3), without any restrictions. A higher ratio of nodes according to this LIN physical layer specification or the one of revision 2.0 will result in a higher transmission reliability.

Figure 3-2. LIN Wake-up Waveform Diagram

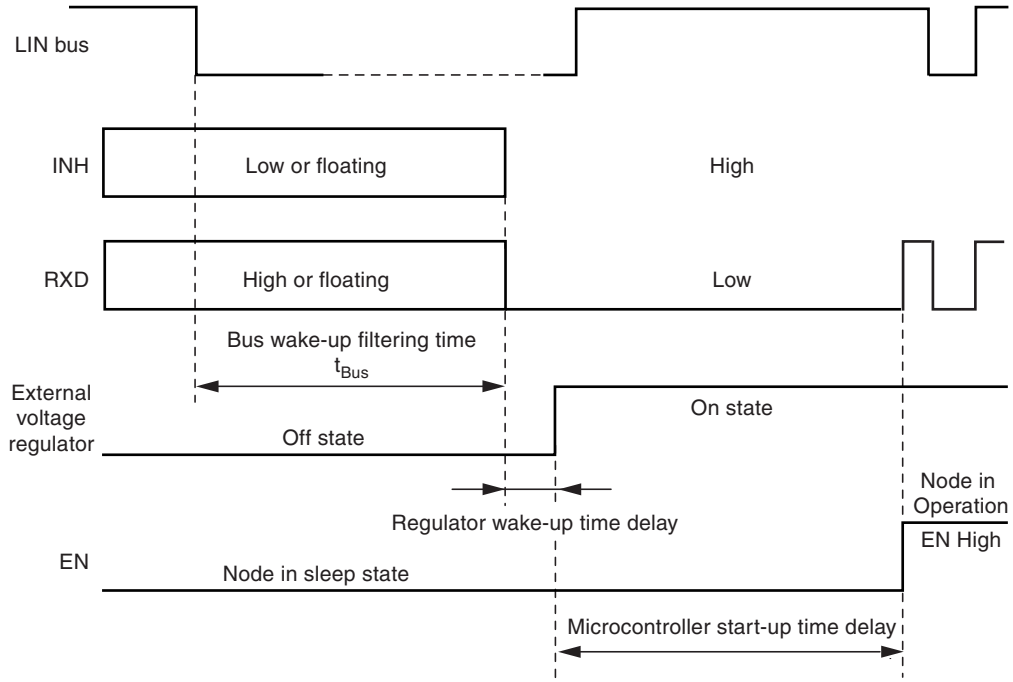
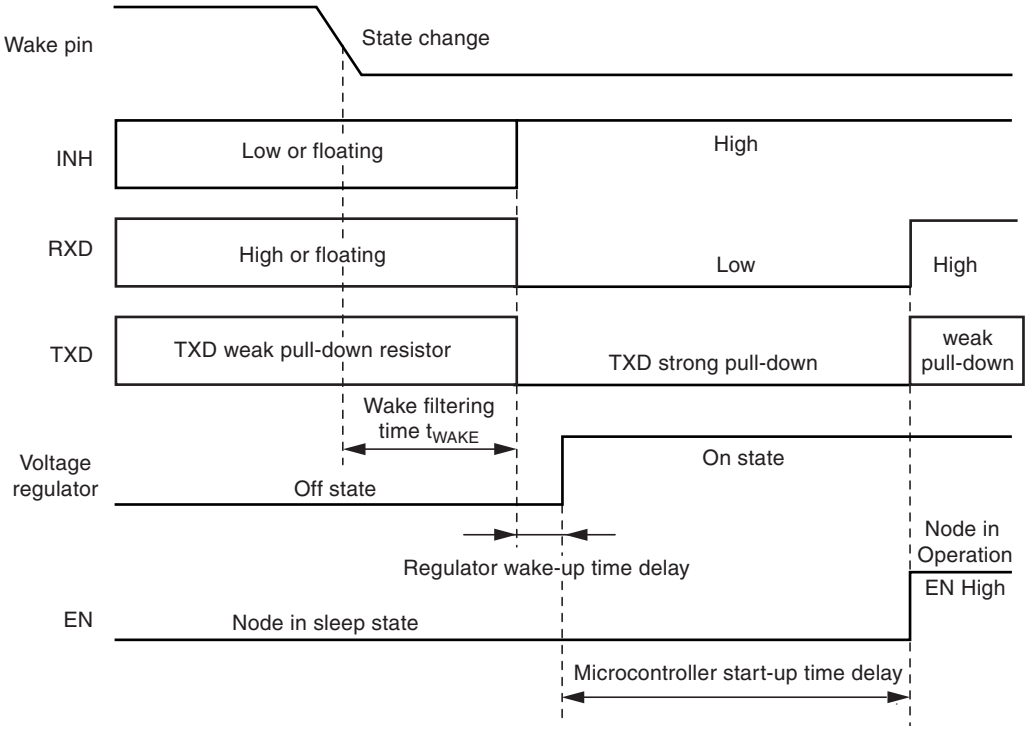


Figure 3-3. LIN Wake-up from Wake-up Switch



4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
V_S - Continuous supply voltage		–0.3		+40	V
Wake DC and transient voltage (with 33 kΩ serial resistor) - Transient voltage due to ISO7637 (coupling 1 nF)		–40 –150		+40 +100	V V
Logic pins (RXD, TXD, EN)		–0.3		+6	V
LIN - DC voltage - Transient voltage due to ISO7637 (coupling 1 nF)		 –40 –150		 +60 +100	 V V
INH - DC voltage		 –0.3		 +40	 V
ESD (DIN EN 61000-4-2) According LIN EMC Test Specification V1.3 - Pin VS, LIN - Pin Wake (with 33 kΩ serial resistor)		 –6000 –5000		 +6000 +5000	 V V
ESD S5.1 - All pins		–3000		+3000	V
CDM ESD STM 5.3.1-1999 - All pins FCDM ESD STM 5.3.1- All pins MM JEDEC A115A - All pins		–500 –1000 –200		+500 +1000 +200	V V V
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_{stg}	–55		+150	°C
Operating ambient temperature	T_{amb}	–40		+125	°C
Thermal shutdown	T_{off}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}	5	10	20	°C

5. Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance junction ambient	R_{thJA}	160	K/W

6. Electrical Characteristics

5V < V_S < 18V, T_{amb} = –40°C to +125°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**V_S Pin**								
1.1	Nominal DC voltage range		7	V_S	5	13.5	18	V	A
1.2	Supply current in sleep mode	Sleep mode $V_{lin} > V_{Batt} – 0.5V$ $V_{Batt} < 14V$	7	I_{VSstby}		10	20	µA	A
1.3	Supply current in normal mode	Bus recessive	7	I_{VSrec}		1.6	3	mA	A
1.4		Bus dominant Total bus load > 500Ω	7	I_{VSdom}		1.6	3	mA	A
1.5	V_S undervoltage threshold			V_{Sth}	4	4.6	5	V	A
1.6	V_S undervoltage threshold hysteresis		7	V_{Sth_hys}		0.2		V	A
2	**RXD Output Pin (Open Drain)**								
2.1	Low level input current	Normal mode V_{LIN} = 0V, V_{RXD} = 0.4V	1	I_{RXDL}	2	5	8	mA	A
2.2	RXD saturation voltage	5 kΩ pull-up resistor to 5V	1	$Vsat_{RXD}$			0.4	V	A
2.3	High level leakage current	Normal mode $V_{LIN} = V_{BAT}$, V_{RXD} = 5V	1	I_{RXDH}	–3		+3	µA	A
2.4	ESD zener diode	I_{RXD} = 100 µA	1	VZ_{RXD}	6.1		8.6	V	A
3	**TXD Input Pin**								
3.1	Low level voltage input		4	V_{TXDL}	–0.3		+0.8	V	A
3.2	High level voltage input		4	V_{TXDH}	2		6	V	A
3.3	Pull-down resistor	V_{TXD} = 5V	4	R_{TXD}	125	250	600	kΩ	A
3.4	Low level leakage current	V_{TXD} = 0V	4	I_{TXD}	–3		+3	µA	A
3.5	Low-level input current at local wake-up request	Pre-normal mode $V_{LIN} = V_{BAT}$; V_{WAKE} = 0V	4	$I_{TXDwake}$	2	5	8	mA	A
4	**EN Input Pin**								
4.1	Low level voltage input		2	V_{ENL}	–0.3		+0.8	V	A
4.2	High level voltage input		2	V_{ENH}	2		6	V	A
4.3	Pull-down resistor	V_{EN} = 5V	2	R_{EN}	125	250	600	kΩ	A
4.4	Low level input current	V_{EN} = 0V	2	I_{EN}	–3		+3	µA	A
4.5	Enable negative slope for go to sleep	Negative slope V_{EN} = 2V to 0.8V	2	$Slope_{EN}$			60	µs	A
5	**INH Output Pin**								
5.1	High level voltage	Normal mode I_{INH} = –200 µA	8	V_{INHH}	$V_S – 0.8$		V_S	V	A
5.2	High level leakage current	Sleep mode V_{INH} = 27V, V_{Batt} = 27V	8	I_{INHL}	–3		+3	µA	A
6	**WAKE Pin**								
6.1	High level input voltage		3	V_{WAKEH}	V_S – 1V		V_S + 0.3V	V	A
6.2	Low level input voltage	I_{WAKE} = Typically –3 µA	3	V_{WAKEL}	–27V		V_S – 3V	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

6. Electrical Characteristics (Continued)

5V < V_S < 18V, T_{amb} = –40°C to +125°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
6.3	Wake pull-up current	V_S < 27V	3	I_{WAKE}	–30	–10		µA	A
6.4	High level leakage current	V_S = 27V, V_{WAKE} = 27V	3	I_{WAKE}	–5		+5	µA	A
7	**LIN Bus Driver**								
7.1	Driver recessive output voltage	R_{LOAD} = 500Ω/1 kΩ	6	V_{BUSrec}	0.9 × V_S		V_S	V	A
7.2	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VS} = 7V, R_{load} = 500Ω	6	$V_{\_LoSUP}$			1.2	V	A
7.3	Driver dominant voltage $V_{BUSdom\_DRV\_HiSUP}$	V_{VS} = 18V, R_{load} = 500Ω	6	$V_{\_HiSUP}$			2	V	A
7.4	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VS} = 7V, R_{load} = 1000Ω	6	$V_{\_LoSUP\_1k}$	0.6			V	A
7.5	Driver dominant voltage $V_{BUSdom\_DRV\_HiSUP}$	V_{VS} = 18V, R_{load} = 1000Ω	6	$V_{\_HiSUP\_1k\_}$	0.8			V	A
7.6	Pull-up resistor to V_S	The serial diode is mandatory	6	R_{LIN}	20	30	60	kΩ	A
7.7	Self-adapting current limitation V_{BUS} = V_{BAT_max}	T_j = 125°C T_j = 27°C T_j = –40°C	6	I_{BUS_LIM}	52 100 150		110 170 230	mA mA mA	A
7.8	Input leakage current at the receiver, inclusive pull-up resistor as specified	Input leakage current Driver off V_{BUS} = 0V, V_{Batt} = 12V	6	$I_{BUS\_PAS\_dom}$	–1			mA	A
7.9	Leakage current LIN recessive	Driver off 8V < V_{BAT} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{BAT}$	6	$I_{BUS\_PAS\_rec}$		15	20	µA	A
7.10	Leakage current at ground loss, Control unit disconnected from ground, Loss of local ground must not affect communication in the residual network	GND_{Device} = V_S V_{BAT} =12V 0V < V_{BUS} < 18V	6	$I_{BUS\_NO\_gnd}$	–10	+0.5	+10	µA	A
7.11	Node has to sustain the current that can flow under this condition, bus must remain operational under this condition	V_{BAT} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	6	I_{BUS}		0.5	3	µA	A
8	**LIN Bus Receiver**								
8.1	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2	6	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	A
8.2	Receiver dominant state	V_{EN} = 5V	6	V_{BUSdom}	–27		0.4 × V_S	V	A
8.3	Receiver recessive state	V_{EN} = 5V	6	V_{BUSrec}	0.6 × V_S		40	V	A
8.4	Receiver input hysteresis	V_{HYS} = V_{th_rec} – V_{th_dom}	6	V_{BUShys}	0.028 × V_S	0.1 × V_S	0.175 × V_S	V	A
8.5	Wake detection LIN High level input voltage		6	V_{LINH}	V_S – 1V		V_S + 0.3V	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

6. Electrical Characteristics (Continued)

5V < V_S < 18V, T_{amb} = –40°C to +125°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.6	Wake detection LIN Low level input voltage	I_{LIN} = Typically –3 µA	6	V_{LINL}	–27V		V_S – 3V	V	A
8.7	LIN pull-up current	V_S < 27V	6	I_{LIN}	–30	–10		µA	A
9	**Internal Timers**								
9.1	Dominant time for wake-up via LIN bus	V_{LIN} = 0V	6	t_{BUS}	30	90	150	µs	A
9.2	Time of low pulse for wake-up via pin WAKE	V_{WAKE} = 0V	3	t_{WAKE}	60	130	200	µs	A
9.3	Time delay for mode change from pre-normal mode to normal mode via pin EN	V_{EN} = 5V	2	t_{norm}	2	10	15	µs	A
9.4	Time delay for mode change from normal mode into sleep mode via pin EN	V_{EN} = 0V	2	t_{sleep}	2	10	12	µs	A
9.5	TXD dominant time out timer	V_{TXD} = 0V	4	t_{dom}	6	9	20	ms	A
9.6	Power-up delay between V_S = 5V until INH switches to high	V_{VS} = 5V		t_{VS}			200	µs	A
10	**LIN Bus Driver (see Figure 6-1 on page 12)** Bus load conditions: Load1 small 1 nF 1 kΩ, Load2 big 10 nF 500Ω, R_{RXD} = 5 kΩ, C_{RXD} = 20 pF; The following two rows specifies the timing parameters for proper operation at 20.0 Kbit/s.								
10.1	Duty cycle 1	$TH_{Rec(max)} = 0.744 \times V_S$ $TH_{Dom(max)} = 0.581 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 50 µs $D1 = t_{bus\_rec(min)}/(2 \times t_{Bit})$	6	D1	0.396				A
10.2	Duty cycle 1	$TH_{Rec(min)} = 0.422 \times V_S$ $TH_{Dom(min)} = 0.284 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 50 µs $D2 = t_{bus\_rec(max)}/(2 \times t_{Bit})$	6	D2			0.581		A
10.3	Slope time falling and rising edge at LIN	Load1/Load2 V_S = 7.3V to 18V	6	t_{Slope_fall} t_{Slope_rise}	3.5		22.5	µs	A
10.4	Symmetry of rising and falling edge	VS = 7.3V $t_{sym} = t_{Slope\_fall} - t_{Slope\_rise}$		t_{sym}	–4		+4	µs	A
11	**Receiver Electrical AC Parameters of the LIN Physical Layer** LIN receiver, RXD load conditions (C_{RXD}): 20 pF, $R_{pull-up}$ = 5 kΩ								
11.1	Propagation delay of receiver (see Figure 6-1 on page 12)	$t_{rec\_pd} = \max(t_{rx\_pdr}, t_{rx\_pdf})$		t_{rx_pd}			6	µs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	$t_{rx\_sym} = t_{rx\_pdr} - t_{rx\_pdf}$		t_{rx_sym}	–2		+2	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 6-1. Definition of Bus Timing Parameter

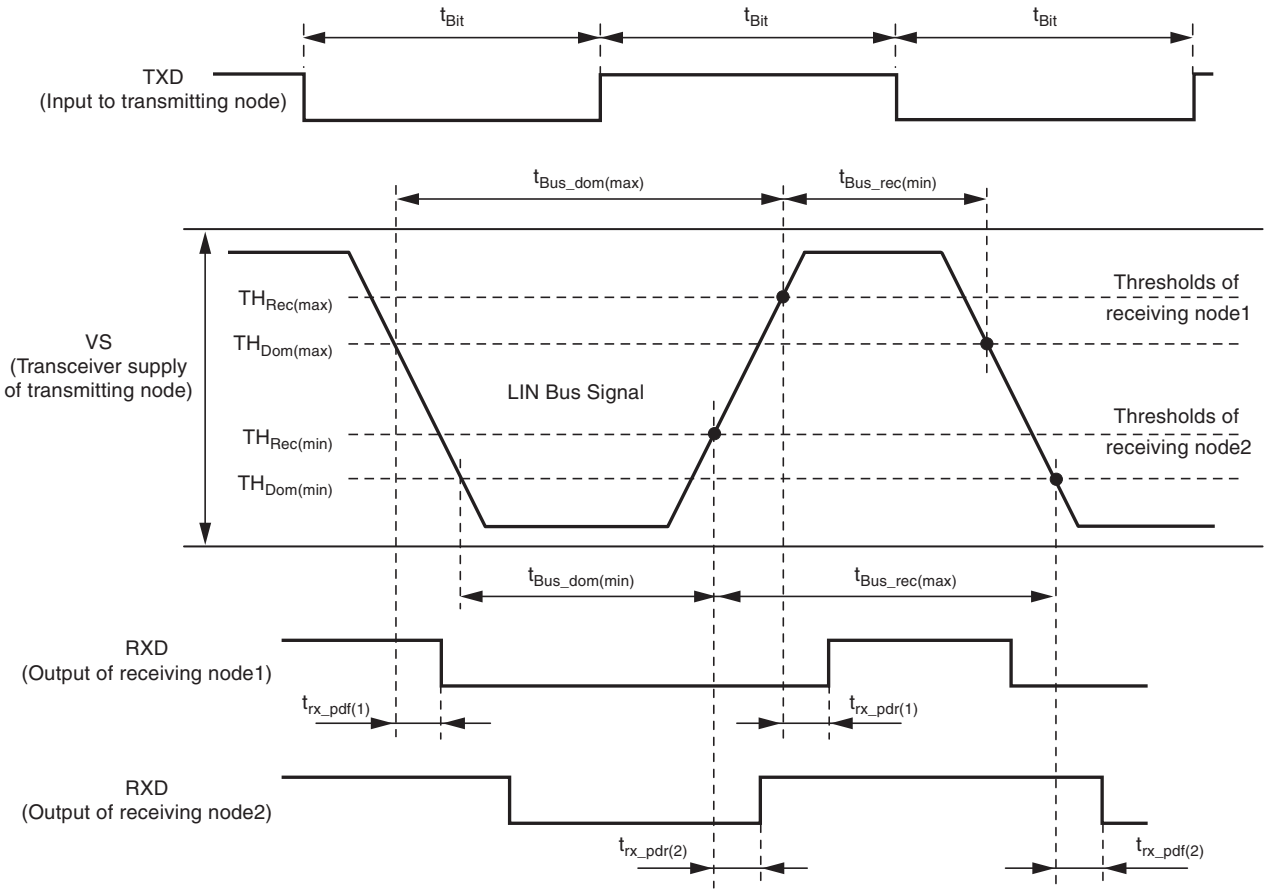
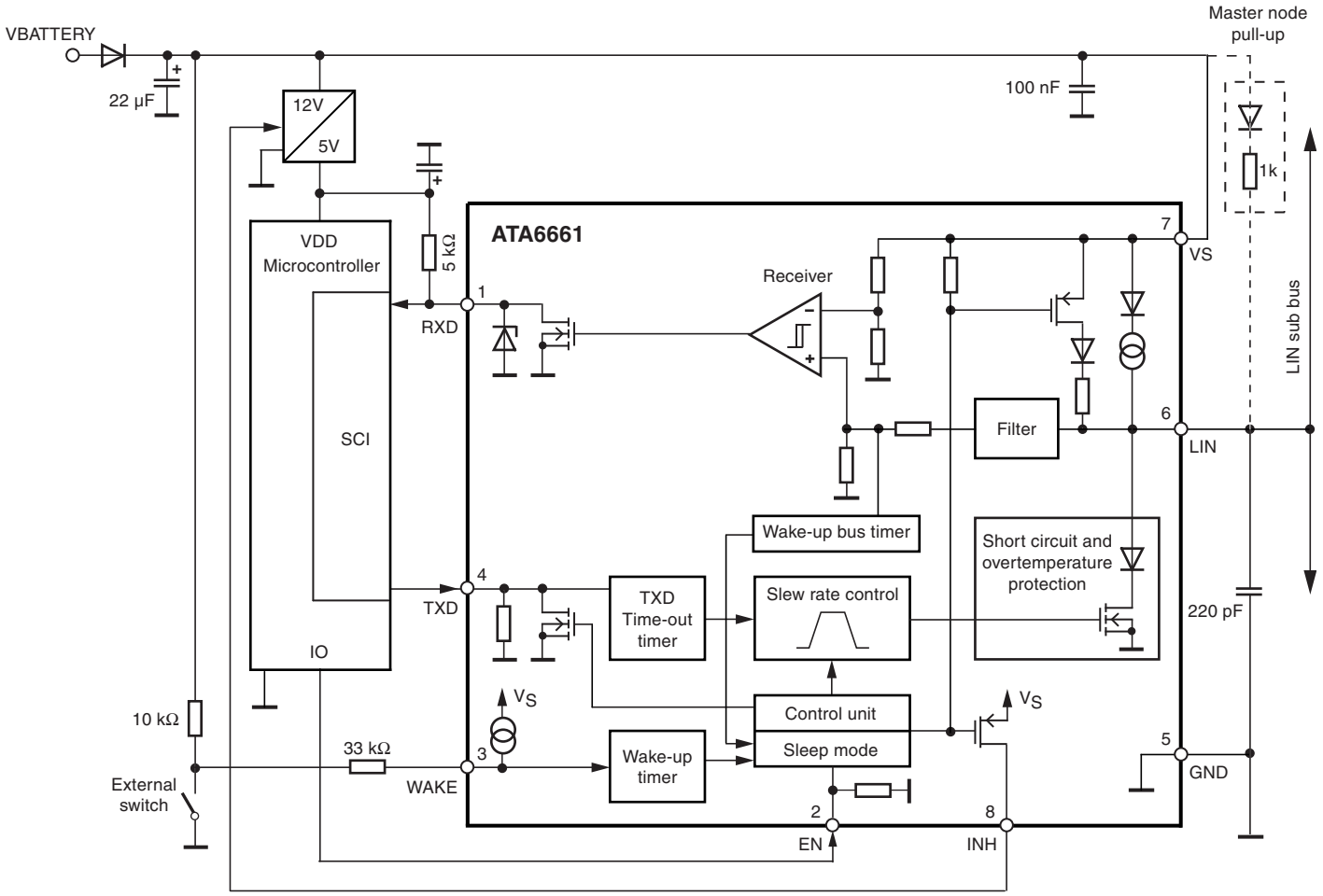


Figure 6-2. Application Circuit



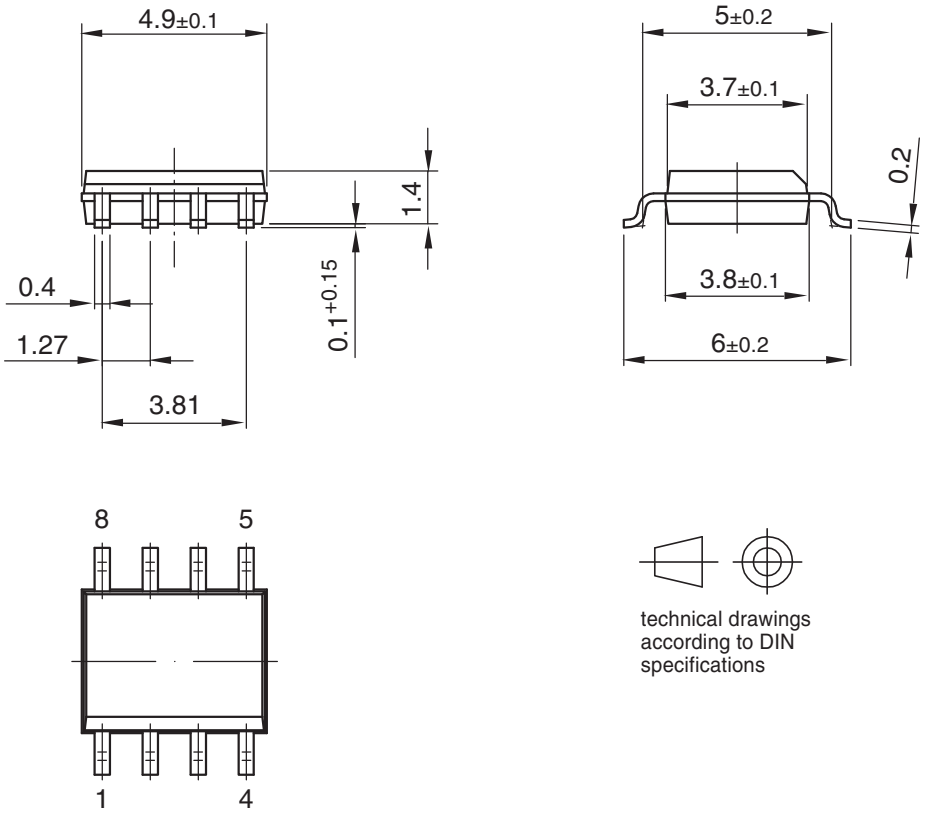
7. Ordering Information

Extended Type Number	Package	Remarks
ATA6661-TAPY	SO8	LIN transceiver, Pb-free, 1k, taped and reeled
ATA6661-TAQJ	SO8	LIN transceiver, Pb-free, 4k, taped and reeled

8. Package Information

Package: SO 8

Dimensions in mm



technical drawings
according to DIN
specifications

Drawing-No.: 6.541-5031.01-4

Issue: 1; 15.08.06

9. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4729M-AUTO-02/09	• Section 6 “Electrical Characteristics” numbers 3.2 and 4.2 on page 9 changed
4729L-AUTO-04/08	• Section 7 “Ordering Information” on page 14 changed
4729K-AUTO-10/07	• Section 7 “Ordering Information” on page 14 changed
4729J-AUTO-07/07	• Put datasheet in a new template • Capital T for time generally changed in a lower case t • Figure 1-1 “Block Diagram” on page 2 changed • Figure 6-2 “Application Circuit” on page 13 changed
4729I-AUTO-12/06	• Put datasheet in a new template • Section 3.5 “TXD Dominant Time-out Function” changed • Section 7 “Ordering Information” on page 14 changed
4729H-AUTO-10/06	• Put datasheet in a new template • Pb-free logo on page 1 deleted • Features on page 1 changed • Section 3-10 “Mode of Operation” on page 5 changed • Figure 3-1 “Mode of Operation” on page 6 changed • Section 3.15 “Physical Layer Compatibility” on page 6 added • Section 6 “Electrical Characteristics” number 4.5 on page 9 added • Section 6 “Electrical Characteristics” number 9.5 on page 11 changed • Section 6 “Electrical Characteristics” number 10.3 and 10.4 on page 11 added • Figure 6-2 “Application Circuit” on page 12 changed
4729G-AUTO-10/05	• Pb-free Logo on page 1 added • Table “Ordering Information” on page 13 changed
4729F-AUTO-05/05	• Section 2.14 “Fail-safe Features” on page 5 changed • Figure 2.2 “LIN Wake-up Waveform Diagram” on page 6 changed • Table “Absolute Maximum Ratings” on page 7 changed • Table “Electrical Characteristics”: Rows: 7.1, 7.2, 7.4, 8.5, 9.3 and 9.5 changed
4729E-AUTO-01/05	• Put datasheet in a new template • Table “Ordering Information” on page 13 changed
4729D-AUTO-10/04	• Put datasheet into new template • Section “Features” on page 1 changed • Figure 1 “Block Diagram” on page 1 changed • Section “Bus Pin (LIN)” on page 2 changed • Section “TX Dominant Time-out Function” on page 3 changed • Section “Output Pin (RXD)” on page 3 changed • Section “Inhibit Output Pin (INH)” on page 3 changed • Section “Wake-up Input Pin (WAKE)” on page 3 changed • Section “Remote Wake-up via Dominant Bus State” on page 4 changed • Section “Fail-safe Features” added • Table “Absolute Maximum Ratings” on page 7 changed • Table “Electrical Characteristics”: Rows: 1.3, 1.4, 1.5, 6.2, 7.9, 7.10, 7.11 and 9.3 changed • Table “Electrical Characteristics”: Rows: 2.4, 8.5, 8.6 and 8.7 • Figure 7 “Application Circuit” on page 12 changed
4729C-AUTO-06/04	• Table “Ordering Information” on page 13 changed

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
auto_control@atmel.com

Sales Contact
www.atmel.com/contacts

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